EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	703/1.ccls. and "test vector"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:26
L2	0	703/1.ccls. and "logic cone"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:23
L3	0	703/1.ccls. and "logic corn"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:24
L4	1	703/1.ccls. and "logic verification"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:25
L5	59	703/1.ccls. and logic and verif$7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:26
L6	2	714/1.ccls. and "test vector"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:26
L7	345	"703"/$.ccls. and "test vector"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:26
L8	10	"703"/$.ccls. and "test vector" and ("logic corn" "logic cone")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:28
L9	23	"714"/$.ccls. and "test vector" and ("logic corn" "logic cone")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:28

EAST Search History

L10	21	"716"/$.ccls. and "test vector" and ("logic corn" "logic cone")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/29 14:28
S1	144	circuit adj (design designing generation) and (aparatus method program tool machine device) and @pd < "19990629" and automatic and (storing recording record storage) and logic and (verification verify checking) and unit and (divide dividing) and (changing modification modify change)	USPAT	OR	OFF	2003/12/22 11:10
S2	14	"Logic Cone$" and predetermin$ and @pd < "19990629"	USPAT	OR	ON	2003/11/04 09:17
S3	45	circuit adj (design designing generation) and (aparatus method program tool machine) and pd < "19990629" and automatic and (storing recording record storage save) and logic and (verification verify checking comparing) and unit and (divide dividing split$) and (modif$ chang$ updat$) and @pd>"19950629" and "test$ vector$"	USPAT	OR	OFF	2003/11/14 13:22
S4	16	circuit adj (design designing generation) and (aparatus method program tool machine) and @pd < "19990629" and automatic and (storing recording record storage save) and logic and (verification verify checking comparing) and unit and (divide dividing split$) and (modif$ chang$ updat$) and @pd>"19950629" and "test$ vector$"	USPAT	OR	OFF	2003/11/14 11:26
S5	60	"Logic Cone$"	USPAT	OR	ON	2003/11/14 13:31
S6	320	circuit adj (design designing generation) and (aparatus method program tool machine) and automatic and (storing recording record storage save) and logic and (verification verify checking comparing) and unit and (divid$ split$) and (modif$ chang$ updat$) and @pd>"20000629"	USPAT	OR	OFF	2003/11/14 13:48

EAST Search History

S7	26	circuit adj (design designing generation) and (aparatus method program tool machine) and automatic and (storing recording record storage save) and logic and (verification verify checking comparing) and unit and (divid$ split$) and (modif$ chang$ updat$) and @pd>"20000629" and "test vector"	USPAT	OR	OFF	2003/11/14 14:09
S8	36	circuit$ adj design$ same (apparatus method program tool) and (divid$ split$) and (verif$ debug$ compar$) and (classif$ specif$) and @pd < "19990629" and second and first and (point$ area$) and ("test vector" "testing vectors")	USPAT	OR	OFF	2003/11/14 15:27
S9	91	circuit$ adj design$ same (apparatus method program tool) and (divid$ split$) and (verif$ debug$ compar$) and (classif$ specif$) and second and first and (point$ area$) and ("test vector" "testing vectors")	USPAT	OR	OFF	2003/11/14 15:39
S10	8	circuit$ adj design$ same (apparatus method program tool) and (divid$ split$) and (verif$ debug$ compar$) and (classif$ specif$) and second and "first circuit" and (point$ area$) and ("test vector" "testing vectors")	USPAT	OR	OFF	2003/12/22 07:28
S11	158	"test vector" and circuit and design and (classif$ sort$) and (specif$ demonstrat$ point$) and (model$ specification) and (chang$ modif$ alter$ revis$ correct$) and (unit "step" process$)	USPAT	OR	OFF	2003/12/22 12:50
S12	134	"test vector" and circuit and design and (classif$ sort$) and (specif$ demonstrat$ point$) and (model$ specification descrip$) and (chang$ modif$ alter$ revis$ correct$) and (unit "step" process$) and verif$	USPAT	OR	OFF	2003/12/22 11:37

EAST Search History

S13	53	"test vector" and circuit and design and (classif$ sort$) and (specif$ demonstrat$ point$) and (model$ specification descrip$) and (chang$ modif$ alter$ revis$ correct$) and (unit "step" process$) and verif$ and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 14:39
S14	65	"test vector" and circuit and design and (classif$ sort$) and (specif$ demonstrat$ point$) and (model$ specification) and (chang$ modif$ alter$ revis$ correct$) and (unit "step" process$) and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 13:28
S15	1	"predetermined unit" and "circuit description" and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 14:44
S16	0	"predetermined unit" and ("circuit description" specification) and circuit and HDL and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 14:46
S17	1309	"predetermined unit" and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 14:46
S18	901	"predetermined unit" and circuit and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 15:30
S19	1	"predetermined unit" and circuit and (HDL VHDL) and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 14:46
S20	18	"predetermined unit" and circuit and simulation and (divid$ alter$ modif$ revis$) and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 15:27
S21	336	("test vercor" "test pattern" "testing vector" "testing pattern") and circuit and simulation and (divid$ alter$ modif$ revis$) and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 15:30
S22	218	("test vercor" "test pattern" "testing vector" "testing pattern") and circuit and simulation and (divide dividing divided altered altering alteration alter modification revise revising revised) and (modification modify modifying changed changing change) and (structure specification specify specified model description descriped) and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 15:34

EAST Search History

S23	169	("test vercor" "test pattern" "testing vector" "testing pattern") and circuit and simulation and (divide dividing divided altered altering alteration alter modification revise revising revised) and (modification modify modifying changed changing change) and (structure specification specify specified model description descriped) and logic and @pd < "19990630"	USPAT	OR	OFF	2003/12/22 15:35
S24	105	("test vercor" "test pattern" "testing vector" "testing pattern") and circuit and simulation and (divide dividing divided altered altering alteration alter modification revise revising revised) and (modification modify modifying changed changing change) and (structure specification specify specified model description descriped) and logic and @pd < "19990630" and @pd > "19950101"	USPAT	OR	OFF	2003/12/22 16:49
S25	46	EDA and ATPG and @pd > "19950101"	USPAT	OR	OFF	2003/12/22 15:45
S26	9	EDA and ATPG and @pd < "19990630" and @pd > "19950101"	USPAT	OR	OFF	2003/12/22 15:49
S27	9	EDA and ATPG and @pd < "19990630" and @pd > "19950101" and (test testing tested) and (modification modify modified modifying changing changed changes change alter altering altered) and circuit and (description describe descripped describing model specify specification specified)	USPAT	OR	OFF	2003/12/22 15:53

EAST Search History

S28	144	("test vector" "test pattern" "testing vector" "testing pattern") and circuit and simulation and (divide dividing divided altered altering alteration alter modification revise revising revised) and (modification modify modifying changed changing change) and (structure specification specify specified model description descriped) and logic and @pd < "19990630" and @pd > "19950101"	USPAT	OR	OFF	2003/12/22 16:49
S29	44	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic)	USPAT	OR	ON	2003/12/25 21:08
S30	25	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630"	USPAT	OR	ON	2003/12/25 20:04
S31	25	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630" and ("only" "others not")	USPAT	OR	ON	2003/12/25 20:07
S32	0	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630" and "others not"	USPAT	OR	ON	2003/12/25 20:06

EAST Search History

S33	23	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630" and "only" and ("test vector" "testing vector" "test pattern" "testing pattern" "node" "connection" "point")	USPAT	OR	ON	2003/12/25 20:54
S34	18	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630" and "only" and ("test vector" "testing vector" "test pattern" "testing pattern" "node" "connection" "point") and unit	USPAT	OR	ON	2003/12/25 20:54
S35	0	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630" and "only" and ("test vector" "testing vector" "test pattern" "testing pattern" "node" "connection" "point") and " verif$ unit"	USPAT	OR	ON	2003/12/25 20:55
S36	5	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630" and "only" and ("test vector" "testing vector" "test pattern" "testing pattern" "node" "connection" "point") and verif$	USPAT	OR	ON	2003/12/25 20:56

EAST Search History

S37	5	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and @pd < "19990630" and "only" and ("test vector" "testing vector" "test pattern" "testing pattern" "node" "connection" "point") and verif$ and (unit step process)	USPAT	OR	ON	2003/12/25 20:57
S38	9	("changed point" " "modification" "changed portion" "altered point" "altered portion" modified point" " modified portion" "revised portion" "revised point") and "circuit design" and (apparatus method tool machine machanic) and (divid$3 partion$3 split$3 seperat$3) and verif$7	USPAT	OR	ON	2003/12/25 21:10